

**In the Claims:**

Please amend claims 1-12 and add new claims 19-25 as indicated below. This listing of claims replaces all prior versions.

1. (*Currently amended*) A [[M]]method for manufacturing on a substrate a semiconductor device with a floating-gate and a control-gate, the method comprising the steps of:

first forming isolation zones in a surface of the substrate,  
thereafter depositing a floating gate layer over the substrate and the isolation zones,  
etching the floating gate layer to form forming a the floating gate on the substrate  
between two of the isolation zones,  
thereafter extending the floating gate using conductive spacers, and  
thereafter forming a the control gate over the floating gate and the conductive  
spacers.

2. (*Currently amended*) The [[M]]method according to claim 1, wherein the step of  
forming the floating gate comprises: etching the floating gate layer to form the floating gate  
includes

forming two opposite walls of providing the floating gate on the substrate, the  
floating gate having one of the two opposite walls located above each of the two isolation  
zones, and

forming a recess in each of the two isolation zones, each of the recesses having a  
wall that is substantially in line with one of under the two opposite walls of the floating  
gate, the recesses extending to a depth from the surface of the substrate.

3. (*Currently amended*) The [[M]]method according to claim 2, further comprising:

forming a tunnel oxide layer on the substrate prior to depositing the floating gate  
layer; and

forming a stopping layer on the floating gate layer prior to etching the floating gate  
layer to form the floating gate,

wherein etching the floating gate to form the floating gate includes a first etching  
step that stops on the floating gate layer, a second etching step that stops on the two

isolation zones thereby forming the two opposite walls of the floating gate, and a third etching step that forms the recesses in the two isolation zones.

~~wherein the step of providing the floating gate, comprises:~~

~~—— depositing a floating gate layer, and~~

~~—— forming slits in the floating gate layer, thus forming the opposite walls of the floating gate.~~

4. (Currently amended) The [[M]]method according to claim 2, wherein the step of extending the floating gate comprises includes depositing a conductive layer over the floating gate and in the recesses in the two isolation zones on the opposite walls of the floating gate and on walls of the recesses in the isolation zones.

5. (Currently amended) The [[M]]method according to claim 4, wherein extending the floating gate further includes etching the conductive layer thereby forming the conductive spacers on the step of depositing a conductive layer on the opposite walls of the floating gate and on the walls of the recesses in the two isolation zones comprises:

~~—— depositing a conductive layer over the floating gate and in the recesses in the isolation zones, and~~

~~—— etching the conductive layer.~~

6. (Currently amended) The [[M]]method according to claim 1, further comprising a step of forming a dielectric layer on the floating gate and on the conductive spacers before forming the control gate.

7. (Currently amended) The [[M]]method according to claim 1, wherein the isolation zones are shallow trench isolation (STI) zones.

8. (Currently amended) The [[M]]method according to claim 1, wherein the isolation zones are LOCOS regions.

9. (*Currently amended*) The [[M]]method according to claim 2, wherein [[a]] the recesses  
in an the two isolation zones are is formed by etching.

10. (*Currently amended*) The [[M]]method according to claim 1, further comprising a-step  
of providing a tunnel oxide between the semiconductor substrate and the floating gate.

11. (*Currently amended*) The [[M]]method according to claim 1, wherein ~~the step of~~  
forming the control gate comprises: includes

forming a dielectric layer on the floating gate and the conductive spacers,

depositing a control gate layer on the dielectric layer, and

patterning the control gate layer to form the control gate.

12. (*Currently amended*) The [[M]]method according to claim 1, wherein the conductive  
spacers are polysilicon spacers and the floating gate layer in a polysilicon layer.

Claims 13-18 (*Cancelled*)

19. (*New*) The method according to claim 11, wherein the control gate layer is a polysilicon layer.

20. (*New*) The method according to claim 2, wherein forming the control gate includes  
depositing a control gate layer over the floating gate and the conductive spacers, the  
control gate layer extending into the recesses in the two isolation zones, and  
patterning the control gate layer to form the control gate.

21. (*New*) A method for manufacturing on a substrate a semiconductor device with a  
floating-gate and a control-gate, the method comprising:  
first forming isolation zones in a surface of the substrate;  
thereafter depositing a polysilicon layer over the substrate and the isolation zones;

etching the polysilicon layer to form the floating gate on the substrate between two of the isolation zones, the floating gate having two opposite walls one of which is located above each of the two isolation zones;

thereafter etching the two isolation zones to form a recess in each of the two isolation zones that extends to a depth from the surface of the substrate, each of the recesses having a wall that is substantially in line with one of the two opposite walls of the floating gate;

thereafter extending the floating gate using conductive spacers; and

thereafter forming the control gate over the floating gate and the conductive spacers.

22. (New) The method of claim 21, further comprising:

forming a tunnel oxide layer on the substrate prior to depositing the polysilicon layer; and

forming a stopping layer on the polysilicon layer prior to etching the polysilicon layer to form the floating gate,

wherein etching the polysilicon layer to form the floating gate includes a first etching step that stops on the polysilicon layer and a second etching step that stops on the two isolation zones thereby forming the two opposite walls of the floating gate.

23. (New) The method of claim 21, wherein extending the floating gate includes depositing a conductive layer over the floating gate and in the recesses in the two isolation zones.

24. (New) The method of claim 23, wherein extending the floating gate further includes etching the conductive layer thereby forming the conductive spacers on the opposite walls of the floating gate and on the walls of the recesses in the two isolation zones.

25. (New) The method of claim 21, further comprising forming a dielectric layer on the floating gate and on the conductive spacers before forming the control gate.